

CHIPSETS

Chipset

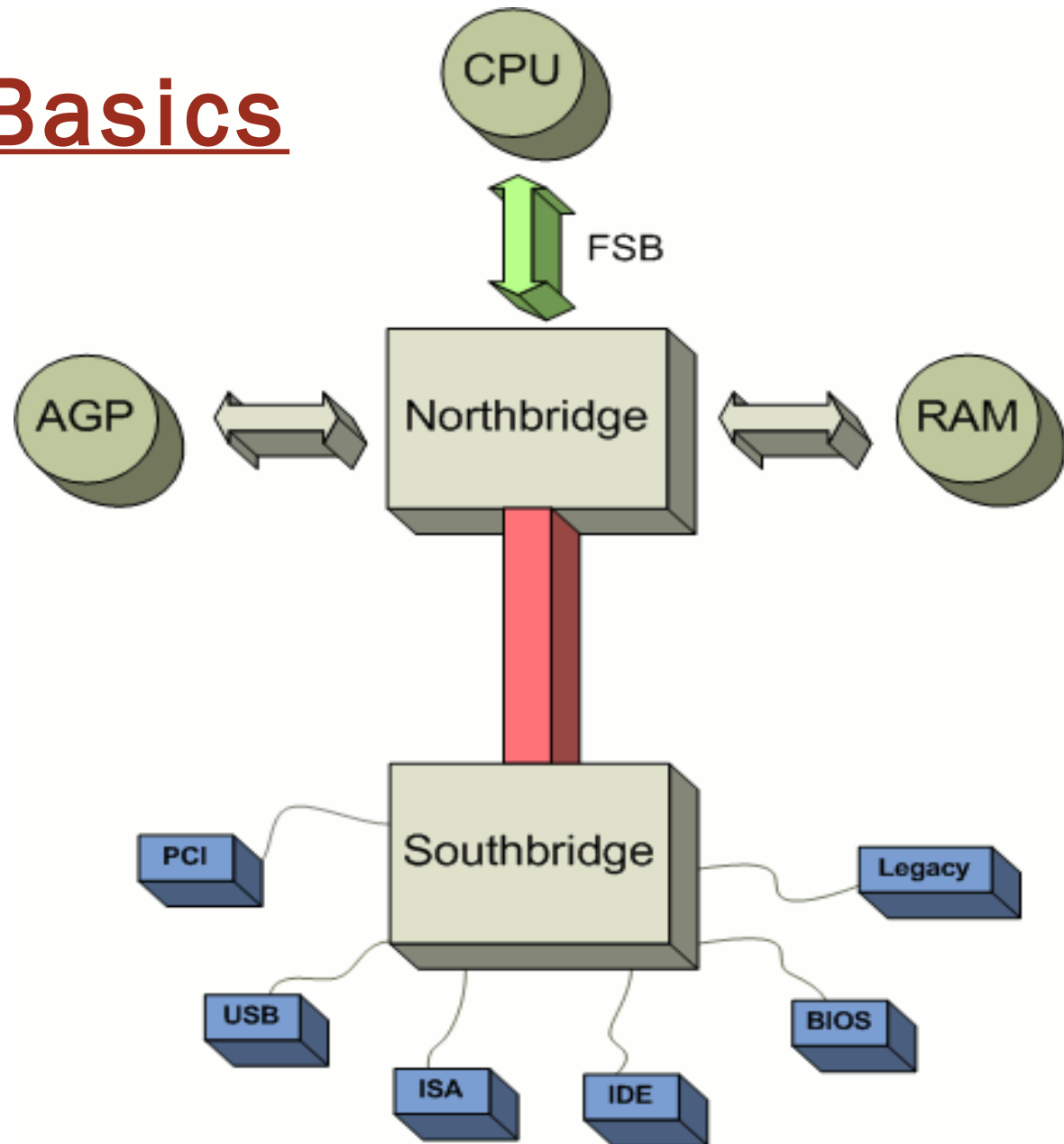
- Motherboard consists of controller chips besides the processor chip
- E.g.:
 - Interrupt Controller
 - DMA controller
 - Timer chip
 - Clock chip
 - Bus Controller chip
 - I/O peripheral interface chip etc..

VLSI chips can perform these functions

CHIPSET

- A Chipset is a group of ICs that are designed to work together and are usually marketed as a single product
- It refers to a set of specialized chips on the motherboard or an expansion card.
- It refers to a pair of chips on the motherboard – *Northbridge and Southbridge*
- A Chipset controls communication between processor and external devices , thus plays an important role in determining system performance

Chipset Basics



Chipset Basics

Northbridge

- Northbridge links the CPU to very high speed devices, especially main memory and graphics controller

Southbridge

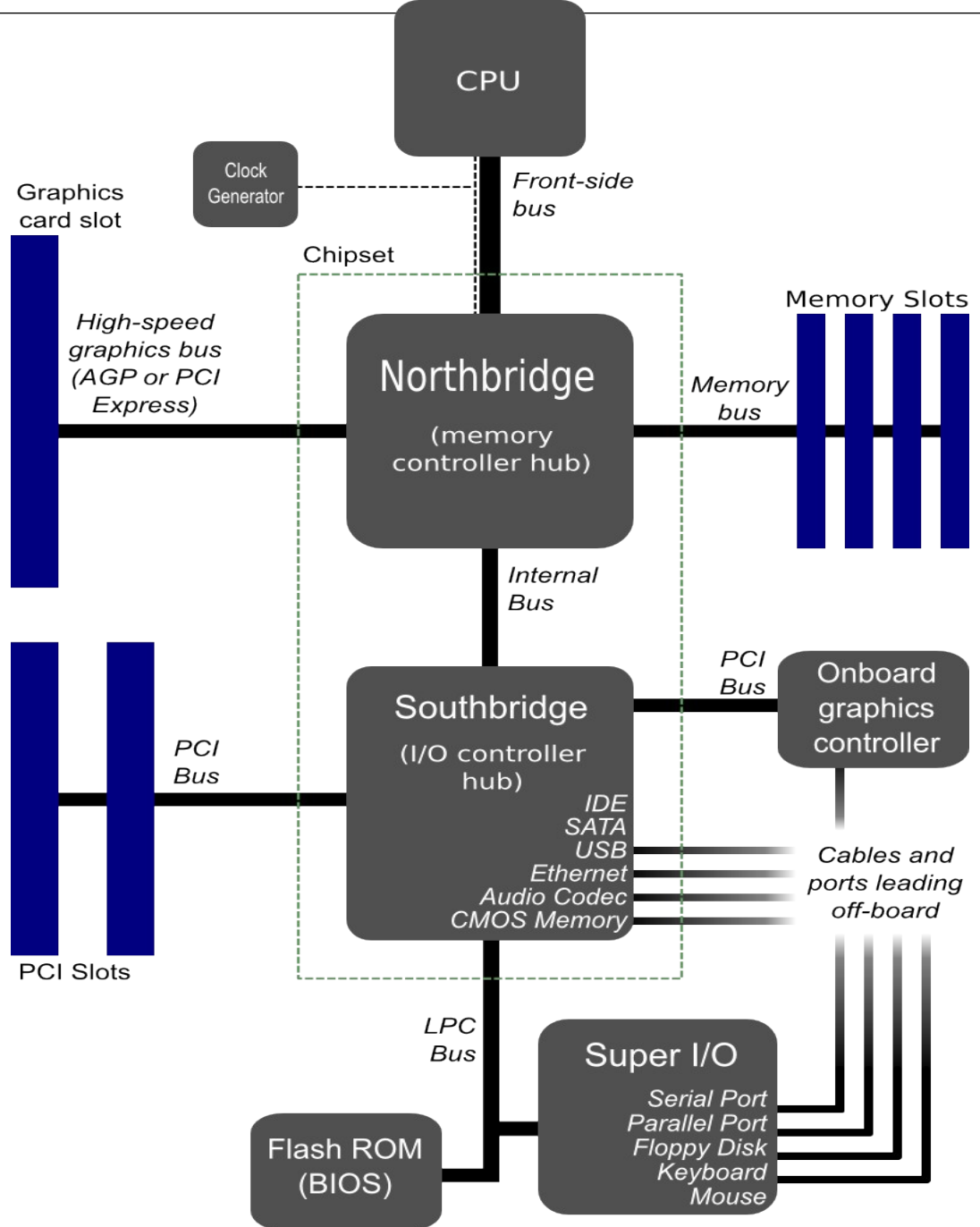
- Southbridge connects to low speed peripheral buses (PCI or ISA).
- The Southbridge actually contains some on Chip integrated peripherals, such as Ethernet, USB and audio devices

Manufacturers

Some of the manufacturers of the chipset are

- NVIDIA
- AMD
- VIA technologies
- SiS
- Intel
- Broadcom

Northbridge-Southbridge Architecture



Functions of NORTHBRIDGE

- Northbridge is also called Memory Controller Hub (MCH) in Intel Systems. It is one of the two chips in the core logic chipset on the PC motherboard.
- There are instances where the two chips are combined onto a single die.
- It handles communication between CPU, RAM, AGP or PCI express and the Southbridge.
- Some Northbridges also have the integrated Video controller called Graphics Memory Controller Hub(GMCH).
- Since different processors and RAM require different signaling, a Northbridge will work with one or two types of CPU and only one type of RAM

Functions of NORTHBRIDGE

- It provides the number, Speed, type of CPU, Size, type of RAM that can be used.
- The Northbridge plays an important role in deciding how far a computer can be over clocked.
- It uses a heat sink and some kind of cooling.
(Fan)

South bridge

- The **Southbridge**, also known as the **I/O Controller Hub (ICH)**
- It is a chip that implements the "slower" capabilities of the motherboard in a Northbridge/Southbridge chipset computer architecture
- It is not directly connected to the CPU. Rather, the Northbridge ties the Southbridge to the CPU.
- A particular type of Southbridge may work with different Northbridge chipsets
- The interface between the Northbridge and the Southbridge is the PCI bus

Southbridge Functionality

The functionality found on a contemporary southbridge includes:

- PCI bus: The PCI bus support includes the traditional PCI specification, but may also include support for PCI-X and PCI Express.
- ISA bus or PLC Bridge: The LPC Bridge provides a data and control path to the Super I/O (the normal attachment for the keyboard, mouse, parallel port, serial port, IR port, and floppy controller) and FWH (firmware hub which provides access to BIOS flash storage).
- SPI bus: The SPI bus is a simple serial bus mostly used for firmware (e.g., BIOS) flash storage access.
- SMBus: The SMBus is used to communicate with other devices on the motherboard (e.g. system fans).

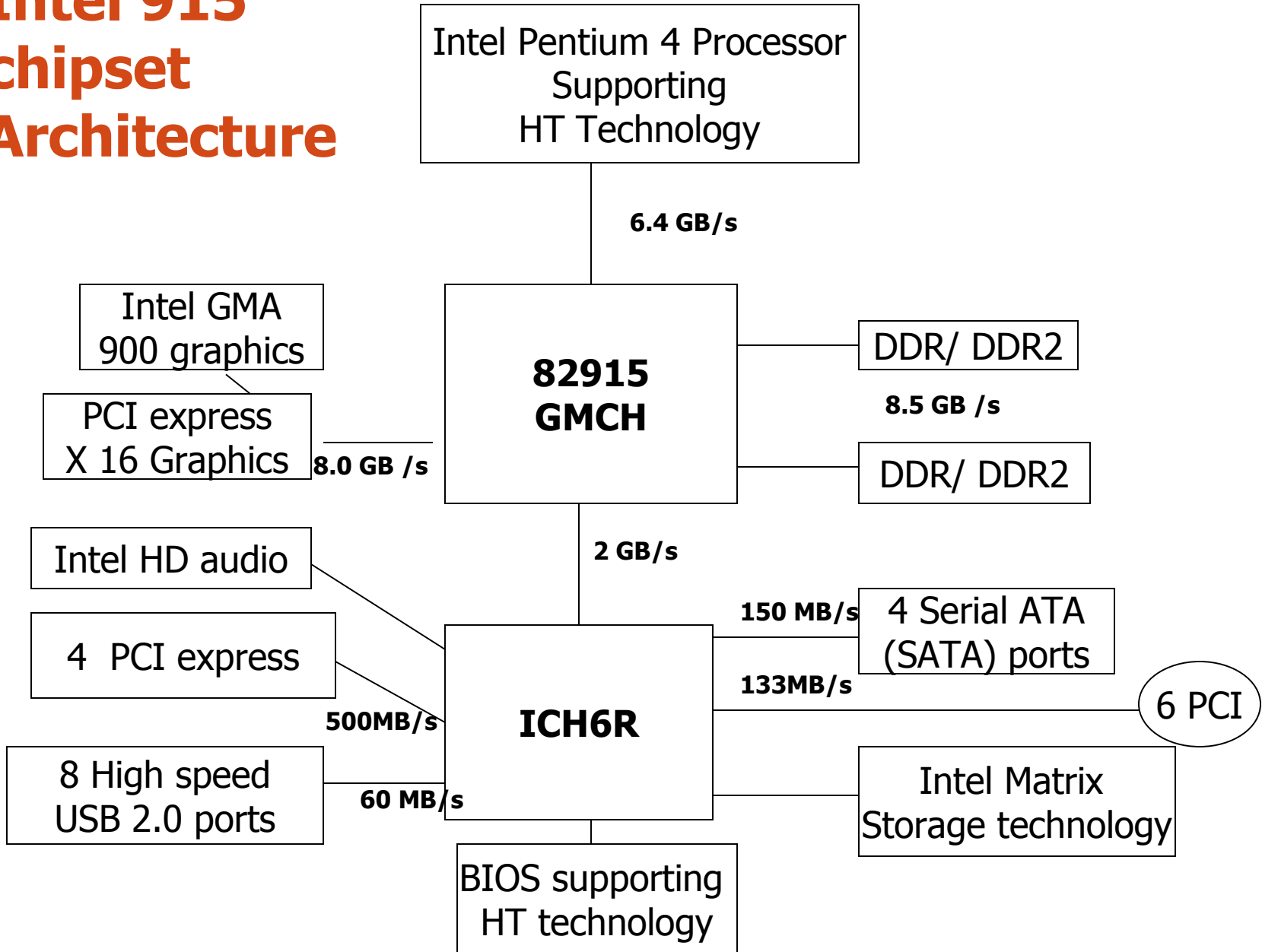
Southbridge Functionality

- DMA controller: The DMA controller allows ISA or LPC devices direct access to main memory without needing help from the CPU.
- Interrupt controller: The interrupt controller provides a mechanism for attached devices to get attention from the CPU
- IDE (SATA or PATA) controller: The IDE interface allows direct attachment of system hard drives.

Southbridge Functionality

- Real Time Clock. The real time clock provides a persistent time account.
- Power management (APM and ACPI). The APM or ACPI functions provide methods and signaling to allow the computer to sleep or shut down to save power.
- Nonvolatile BIOS memory. The system CMOS, assisted by battery supplemental power, creates a limited non-volatile storage area for system configuration

Intel 915 chipset Architecture



Intel 945 chipset Architecture

